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GB 1326758
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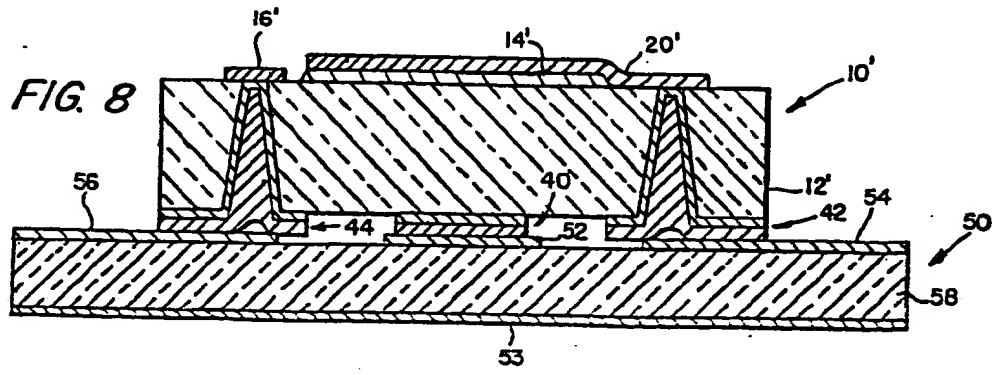
Reddie & Grose

(54) Semiconductor device

(57) A field effect transistor device comprises a semiconductor layer 14' on a semi-insulating substrate 12'. Source, gate 16' and drain 20' electrodes have portions extending over the layer 14' and contacts 40 (source), 42 (drain) and 44 (gate) to all three electrodes xtend through the substrate so that the transistor device can be mounted directly on a microstrip circuit with the gate and drain contacts connected to microstrip conductors 56 and 54 and the source contact connected via conductor 52 to the ground plane 53 on the underside of the microstrip substrate 58. The use of wire bonding from semiconductor electrodes to microstrip conductors is eliminated.

FIG. 8



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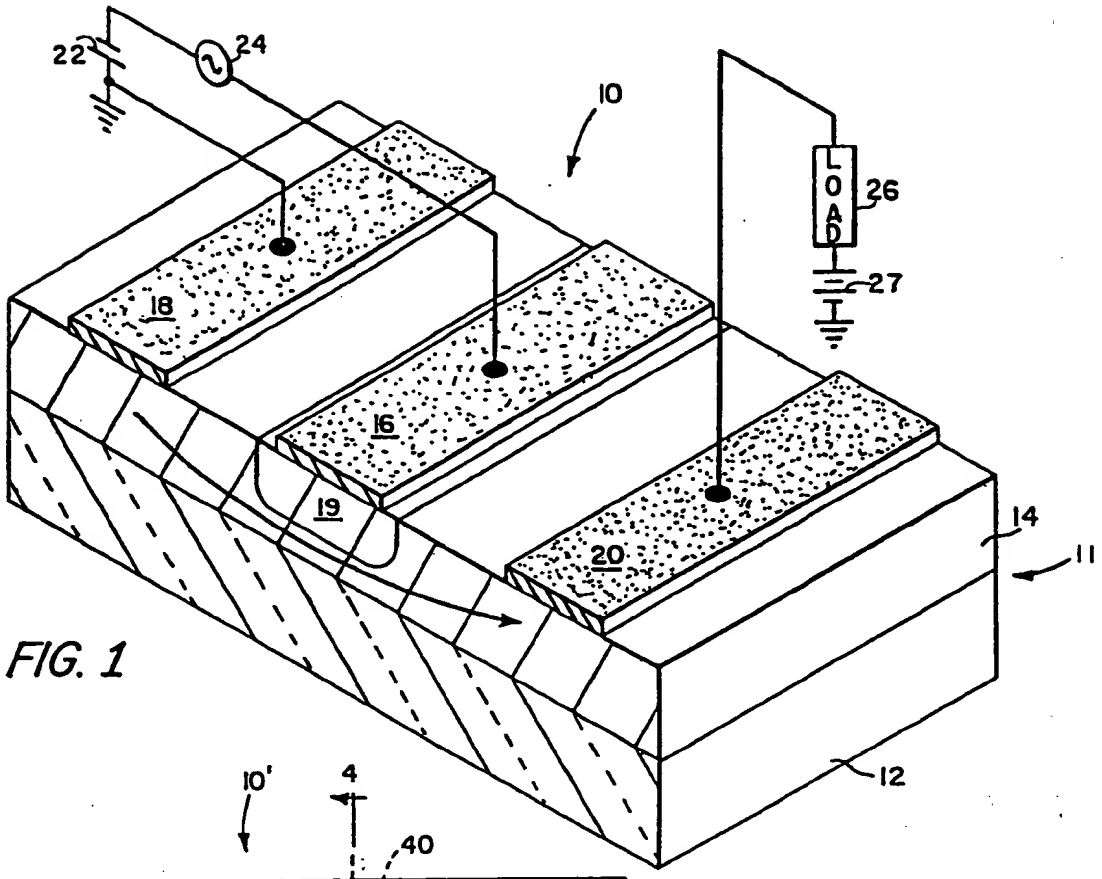


FIG. 1

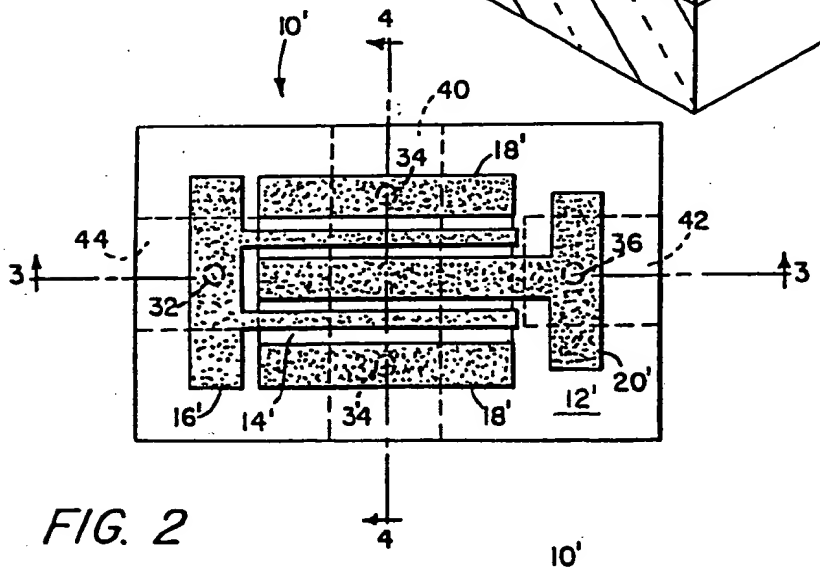


FIG. 2

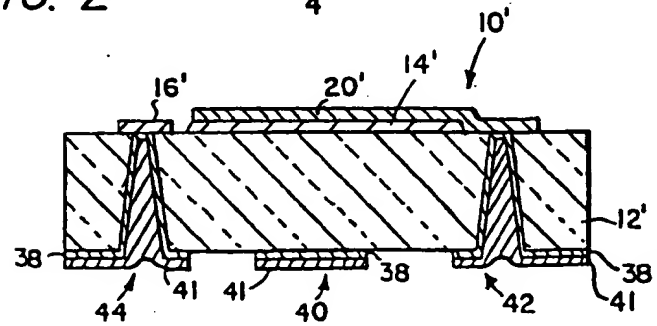


FIG. 3

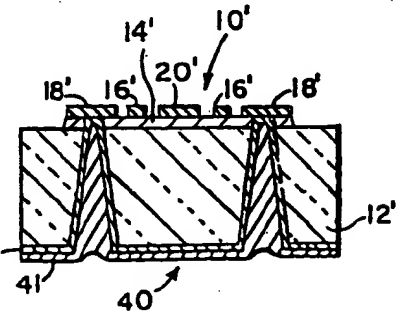


FIG. 4

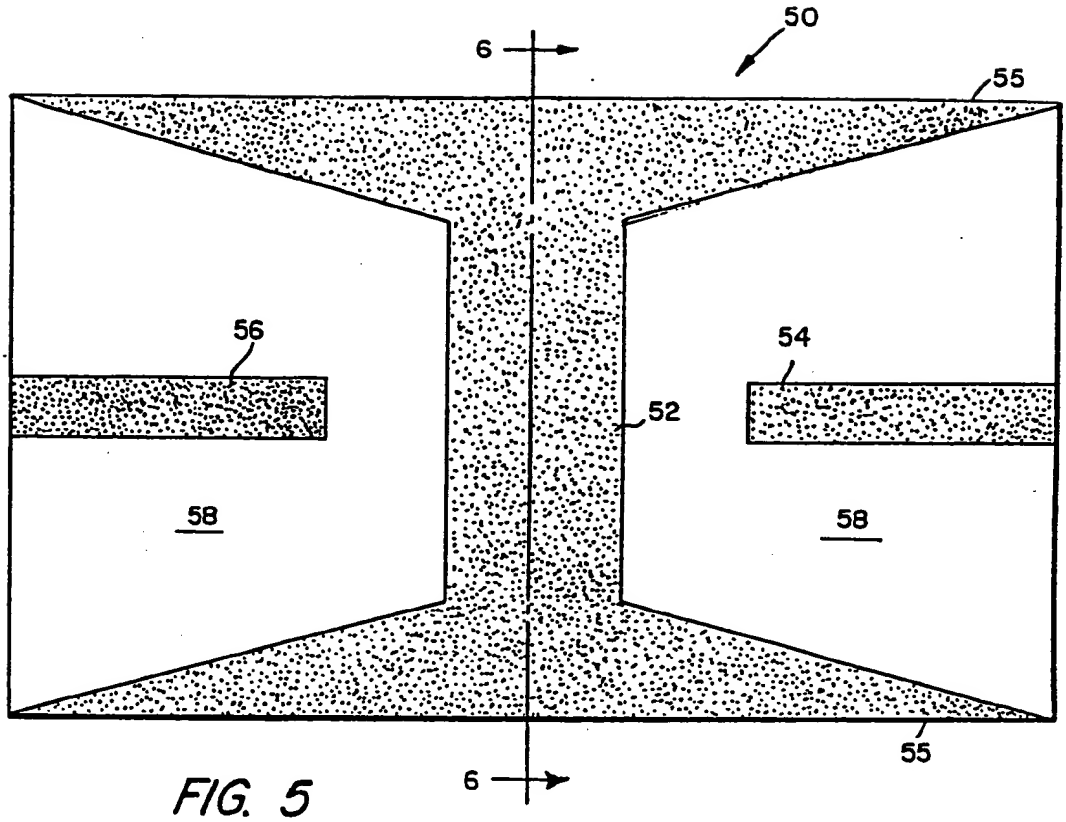


FIG. 5

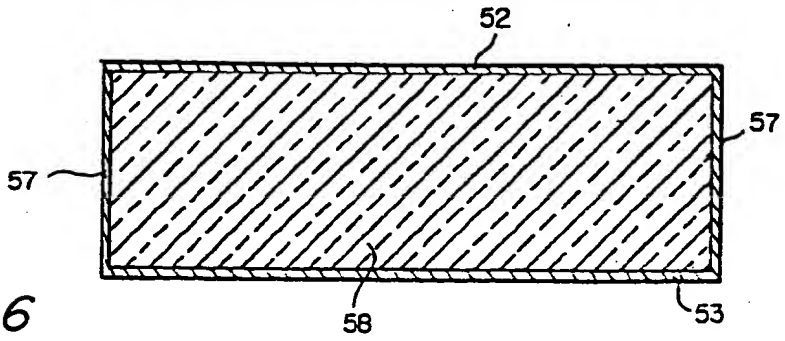


FIG. 6

FIG. 7

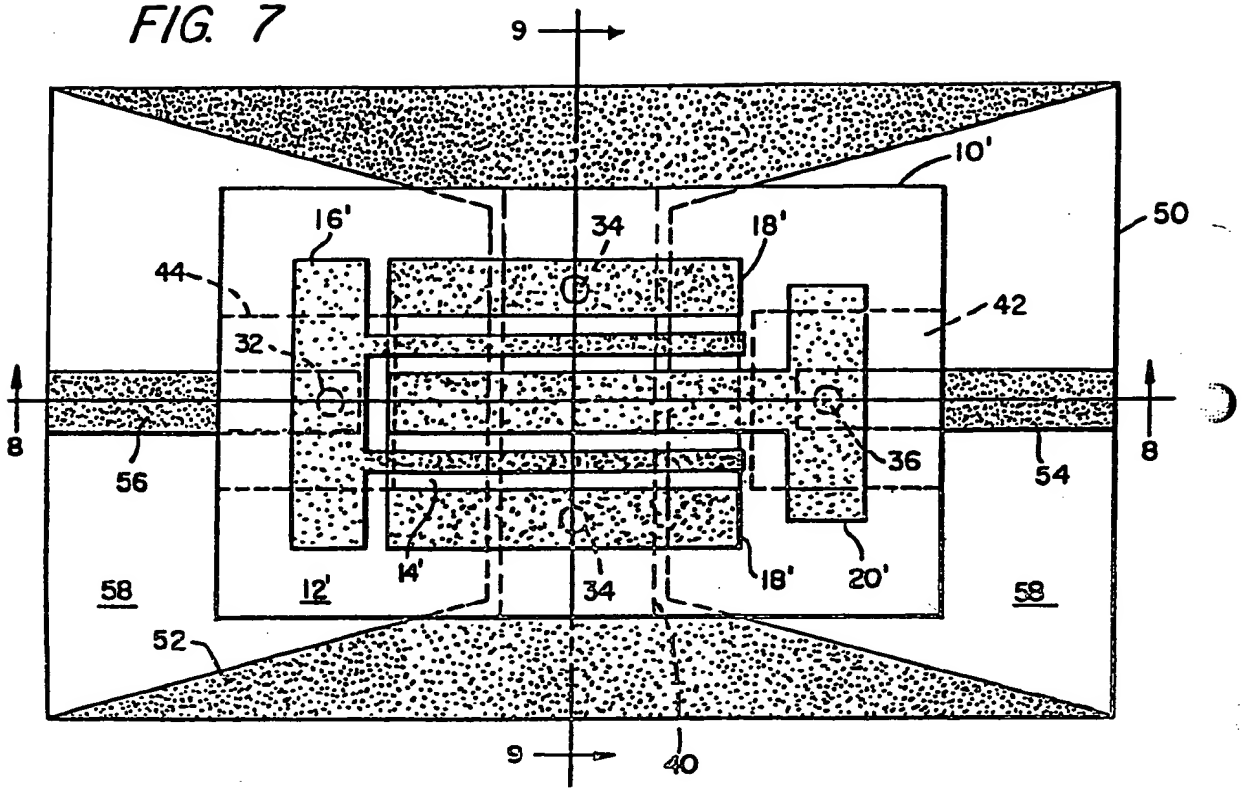


FIG. 8

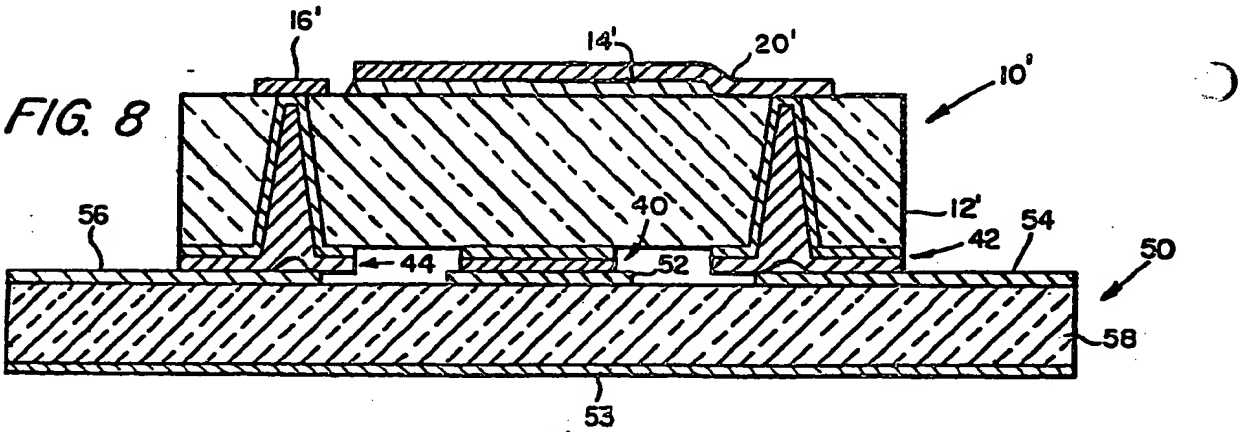
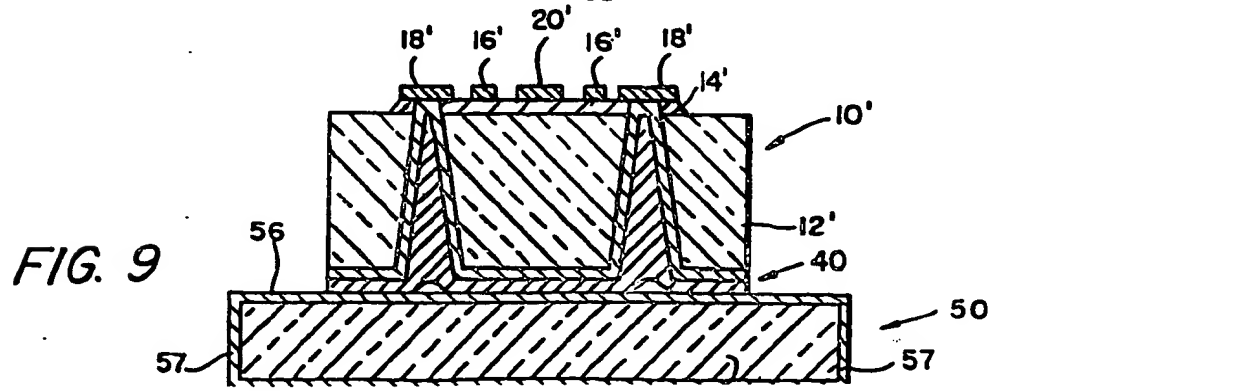


FIG. 9



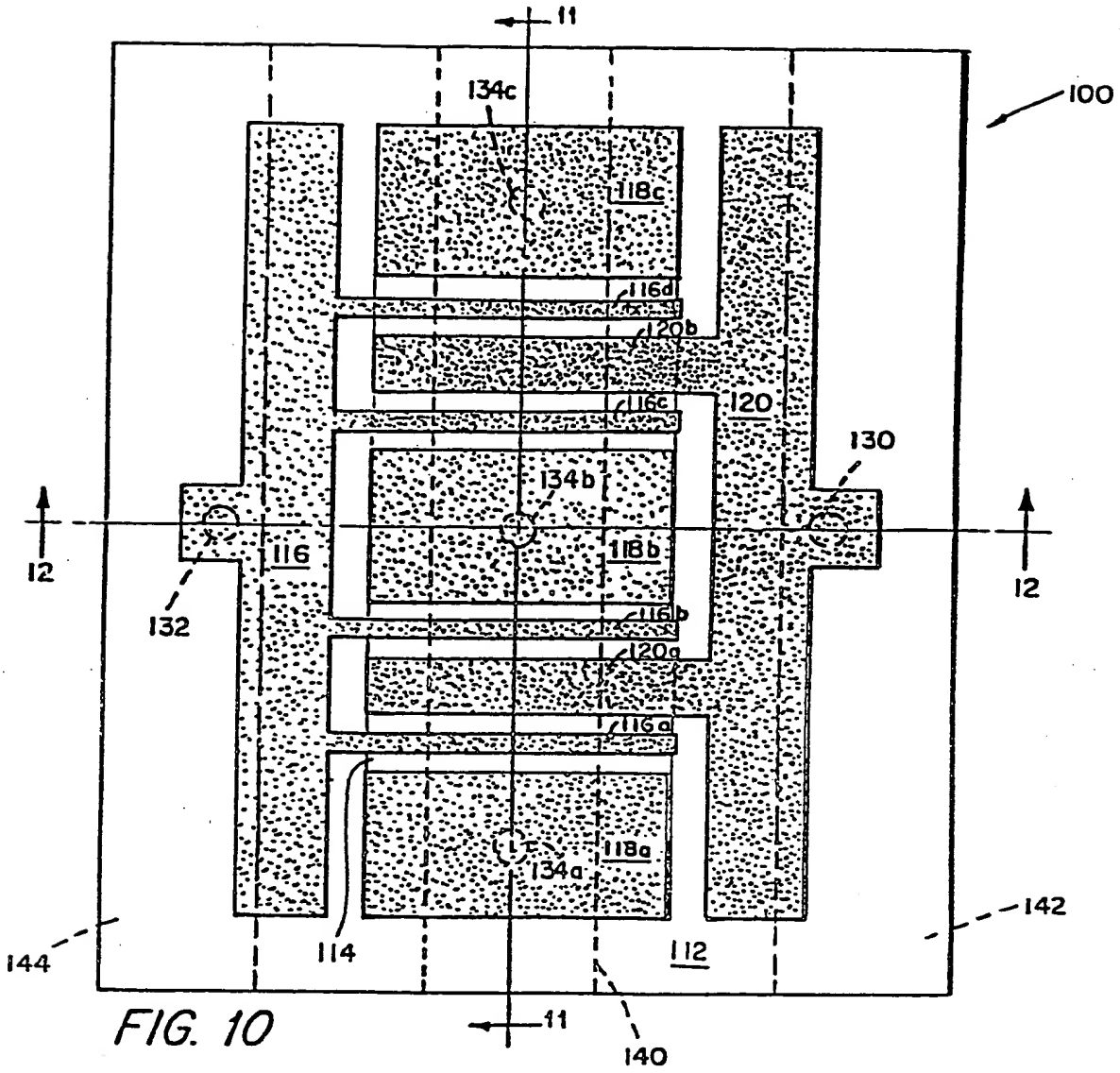

11
134c
100
118c
116d
120b
116c
120
130
134b
12
116
118b
12
132
116b
120a
116a
118a
134a
142
144
114
112
11
140

FIG. 10

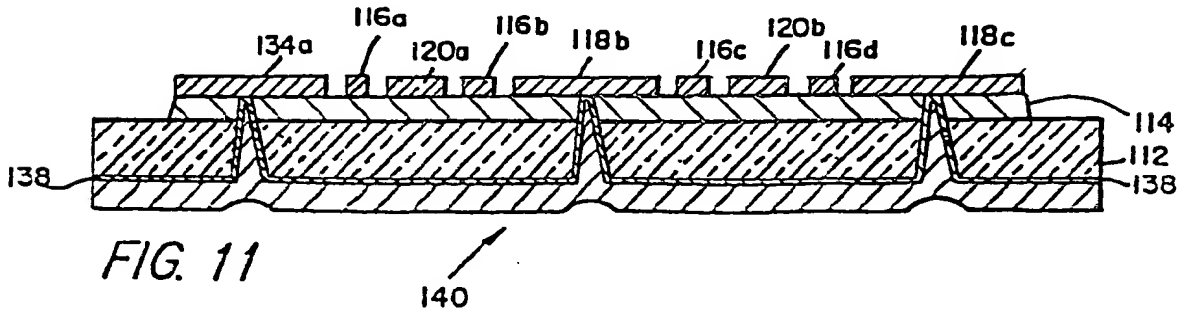
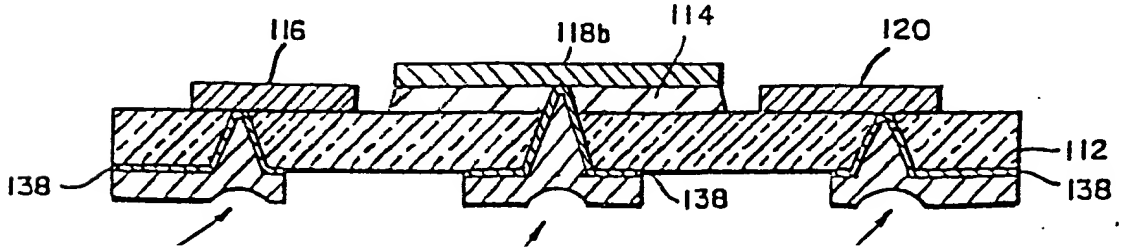

116a
134a
120a
116b
118b
116c
120b
116d
118c
114
112
138
138
140

FIG. 11


116
118b
114
120
112
138
138
138

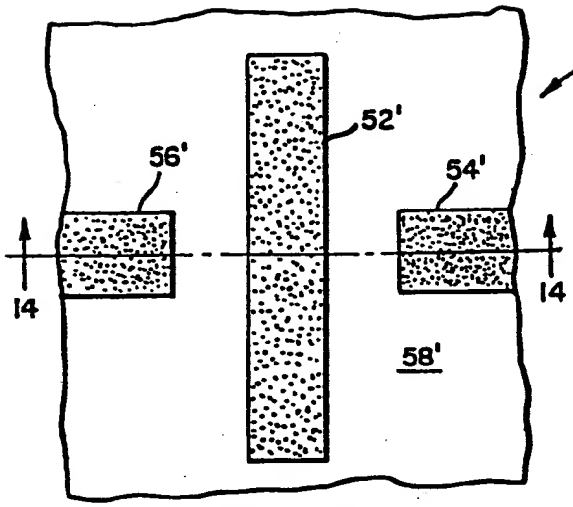


FIG. 13

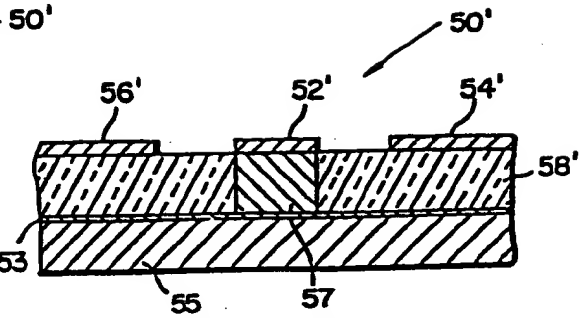


FIG. 14

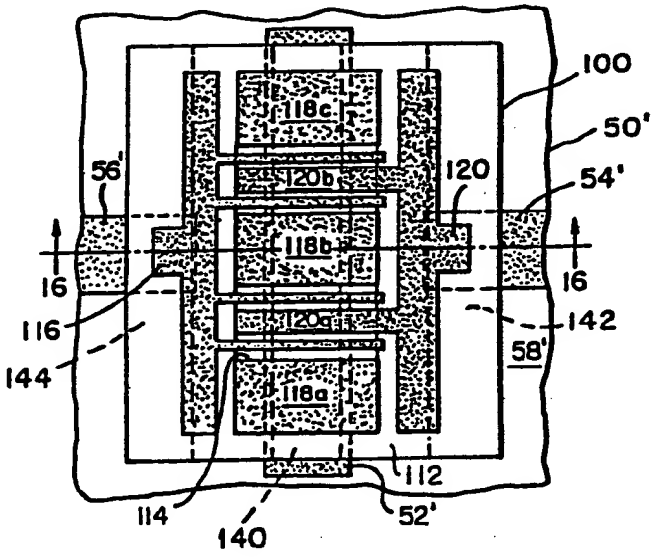


FIG. 15

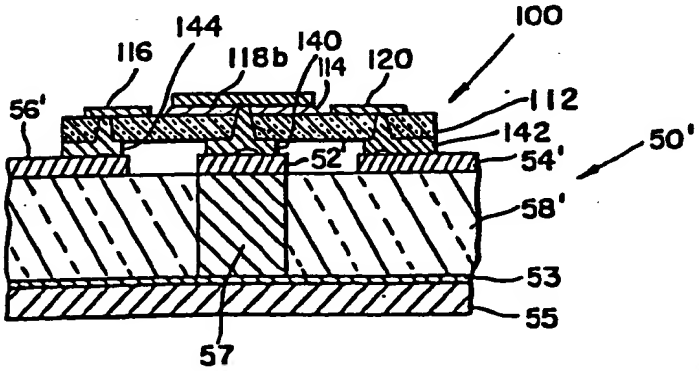


FIG. 16

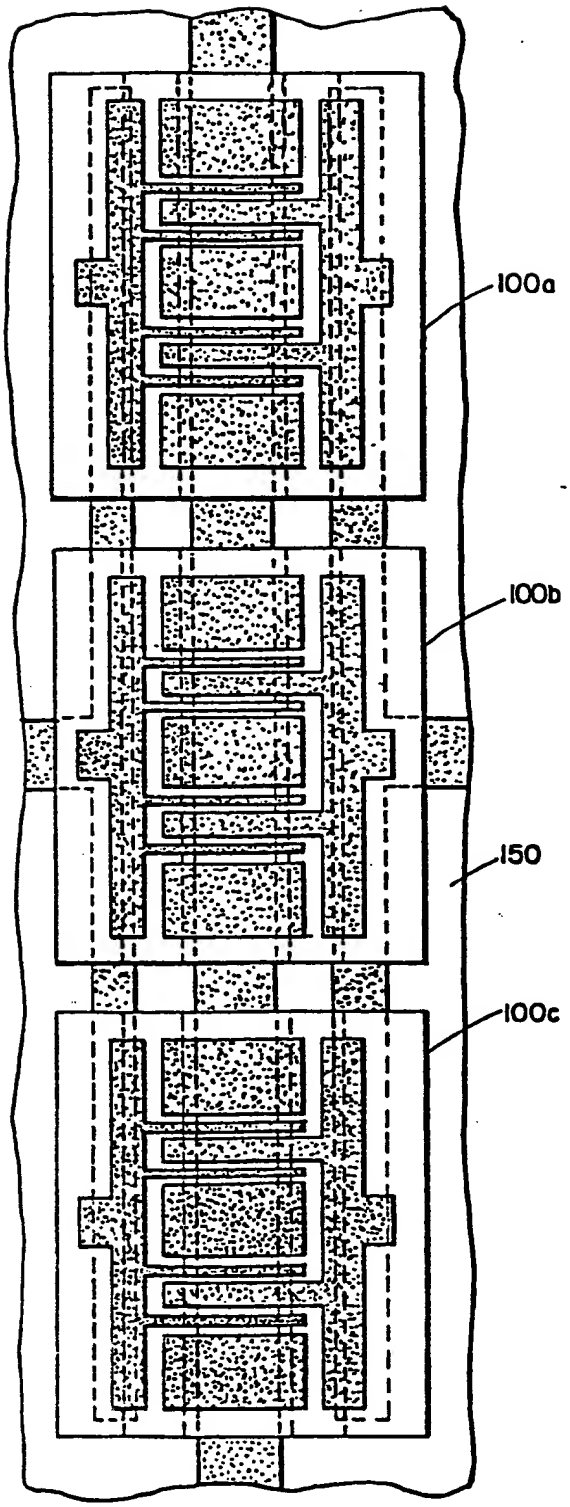


FIG. 17

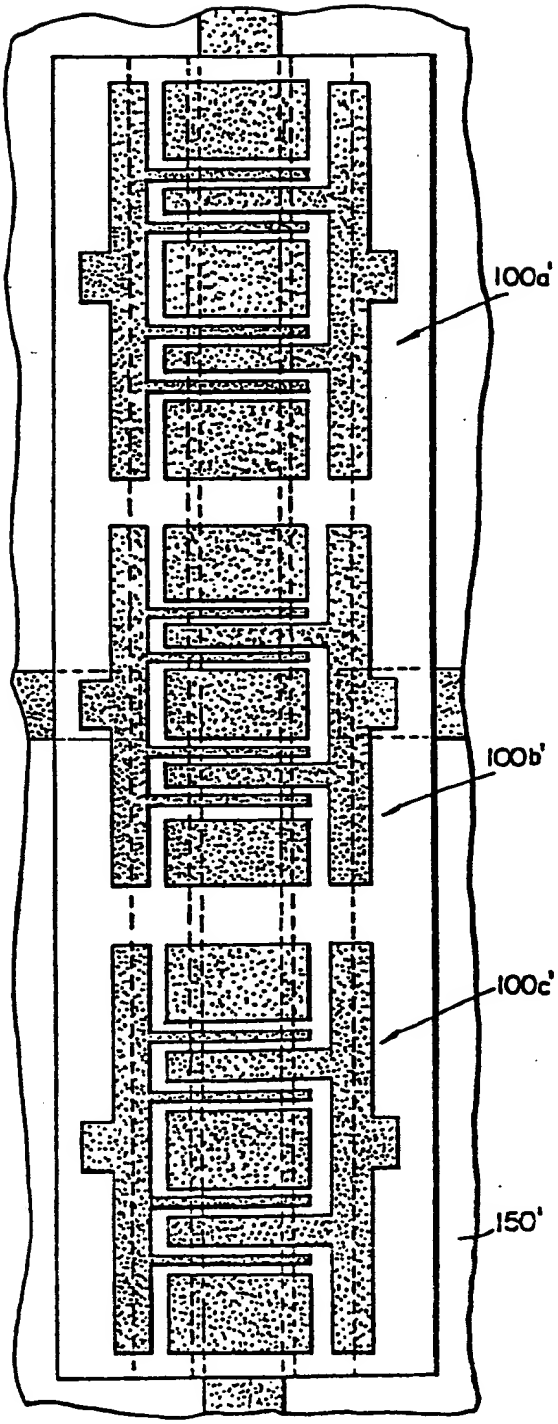


FIG. 18

SPECIFICATION

Semiconductor device

This invention relates generally to semiconductor devices and more particularly to semiconductor devices adapted to operate at microwave frequencies.

As is known in the art, a field effect transistor is a semiconductor device which can be adapted to operate at microwave frequencies. Such a device generally includes a suitable semiconductor, such as gallium arsenide, having formed therein a source region, a drain region and a gate region disposed between the source and drain regions. Source and drain electrodes are formed over a surface of the semicondictor in ohmic contact with the source and drain regions. A gate electrode which is also disposed over the surface of the semiconductor, is, however, formed in rectifying contact with the gate region. The field effect transistor being so formed may then be interconnected with a microstrip circuit by wire bonding the source, drain and gate electrodes to conductors of the microstrip circuit. In another type of field effect transistor, one adapted to operate at relatively high power levels, a plurality of source electrodes has a corresponding one of a plurality of drain electrodes disposed between corresponding pairs of source electrodes. The drain electrodes are interconnected by a suitable conductor formed on an upper surface of the semiconductor. Each one of a plurality of gate electrodes is disposed on the upper surface between a drain electrode and a corresponding one of the source electrodes. The gate electrodes are interconnected by a suitable conductor also formed on the upper surface of the structure. In one type of high power field effect transistor the source electrodes are interconnected by a common conductor formed on the bottom surface of the semiconductor. Each source electrode is connected to the common conductor through a hole filled with a plated metal conductor which passes through the semiconductor to electrically interconnect the source electrode and the common conductor.

In either one of the field effect transistors described the transistor is generally interconnected with a microstrip circuit by wire bonding the drain and gate electrodes to strip conductors of the microstrip circuit. The wire bonding, however, requires that the wire conductors generally pass over, or bridge, air gaps between the edge of the semiconductor and the adjacent edge of the microstrip circuit, th reby causing undesirable impedance mismatching and concomitant radiation of microwav energy. Furtherm re, at microwav frequencies th length of the wire and the position of the bond have significant effects on the electrical characteristics of the field effect transist r-microstrip circuit combination, hence the use of wire bonding requires that, for good reproducibility between devices, both th length of th wir and the position of the bond be substantially the same for all devices requiring matched characteristics. Also, at microwave frequencies the inductance of the wires can cause unwanted parasitic oscillations. Still further, the use of wire b nding generally requires that the device packag be relatively large in order to accommodate the interconnecting wires.

According to the present invention, there is provided, a semiconductor device, comprising a substrate structure including a semiconductor, first and second electrodes in ohmic contact with the semiconductor, a third electrode for controlling the flow of change carriers between the first and second electrodes, and two electrical conductors extending through the substrate structure, each electrical conductor being electrically connected to a corresponding one of two of the first, second and third electrodes.

Preferably a third electrical conductor extends through the substrate structure and is electrically connected to the remaining one of the first, second and third electrodes.

In a microstrip circuit a dielectric substrate is used to support a ground plane conductor and two microstrip conductors, each conductor having a c ntact region disposed on a surface of the dielectric. In a preferred embodiment at least two of the said electrical conductors are disposed on and electrically connected to a corresponding two of the microstrip circuit contact regions.

Because the semiconductor device electrodes are connected directly to the contact regions of the microstrip circuit, mismatches caused by bonding wires across air gaps between the semiconductor device and the dielectric are reduced and spurious oscillations caused by inductive coupling of the wire bonds are eliminated. Furthermore, because wire bonds are not required, the reproducibility of the combined semiconductor device microstrip circuit is improved. Still further, the semiconductor device can be fitted into a smaller package.

The invention will be described, by way of example, with reference to the accompanying drawings, in which:

FIGURE1 is a diagrammatic sketch of a field effect transistor;

FIGURE 2 is a plan view of a field effect device according to the invention;

FIGURE 3 is a cross-sectional view of the field effect device of Figure 2 taken along line 3-3;

FIGURE 4 is a cross-sectional view of the field effect device of Figure 2 taken along line 4-4;

FIGURE 5 is a plan view of a microstrip circuit;

FIGURE 6 is a cross-sectional view of the microstrip circuit of Figure 5 taken along line 6-6;

FIGURE 7 is a plan-view of the field effect device of Figure 2 connected to the microstrip circuit f Figur 5;

FIGURE 8 is a cross-sectional view of the field effect device and connected microstrip circuit of Figure 7 taken along line 8-8;

FIGURE 9 is a cross-sectional view of the field effect transistor and connected microstrip circuit of Figure 7 taken along line 9-9;

FIGURE 10 is a plan view f an alternative embodiment of a field effect device according to th invention;

FIGURE 11 is a cross-sectional view of the field

effect device of Figure 10 taken along line 11-11;

FIGURE 12 is a cross-sectional view of the field effect device of Figure 10 taken along line 12-12;

FIGURE 13 is a plan view of a microstrip circuit;

FIGURE 14 is a cross-sectional view of the microstrip circuit shown in Figure 13 taken along line 14-14;

FIGURE 15 is a plan view of the field effect device of Figure 10 connected to the microstrip circuit of Figure 13;

FIGURE 16 is a cross-sectional view of the field effect device of Figure 10 and connected microstrip circuit of Figure 13 taken along line 16-16 of Figure 15;

FIGURE 17 is a plan view of an alternative embodiment of the invention wherein a plurality of field effect devices of the type shown in Figure 10 are connected to a microstrip circuit; and

FIGURE 18 is another alternative embodiment of the invention wherein a plurality of field effect devices are formed on a common substrate and are connected to a microstrip circuit.

Referring now to Figure 1, a diagrammatic sketch is shown of a field effect transistor (FET) 10 having a single crystal substrate 12, here a gallium arsenide, semi-insulating substrate on which is grown an epitaxial semiconductor layer 14 of n-type conductivity gallium arsenide. Gate, source and drain electrodes 16, 18, 20 are formed on a surface of the semiconductor layer 14. The source and drain electrodes 18, 20 are in ohmic contact with the semiconductor layer 14. The gate electrode 16 forms a rectifying metal-semiconductor contact, or Schottky barrier, with the semiconductor layer 14, rather than being in ohmic contact with such layer 14. Because the gate electrode 16 forms a Schottky barrier with the semiconductor layer 14, the portion 19 of the n-type semiconductor layer 14 under the gate electrode 16, is depleted of electrons when a negative voltage from a supply 22 is applied between the source and gate electrodes 18, 16. The depth of this electron depleted zone (i.e. the depletion zone) increases as the reverse bias voltage 22 increases. By superimposing a signal voltage on the gate electrode 16, as from a suitable R.F. (radio frequency) source 24, here in the microwave band, a modulation of the depth of the depletion zone is produced. (It is also noted that such modulation also modulates the height of the conducting region below the gate electrode, sometimes referred to as the channel.) Because of the modulation in the depth of the depletion zone and the corresponding modulation of the cross-sectional area presented to electron flow, the source drain current (indicated by the arrow) is modulated. Since the gate electrode 16 is reverse-biased a high impedance is presented to the modulating signal. The drain electrode is connected to a load 26 through a supply 27, as shown.

Referring now to Figures 2, 3 and 4, a field effect transistor 10' is shown to include a substrate structure 11 (Figure 1) having a semi-insulating, gallium arsenide, single crystal substrate 12' and an epitaxially grown, n-type conductivity, gallium arsenide semiconductor layer 14', as shown. The semiconductor layer 14' provides the active region for the transistor 10'. The resistivity of the substrate 12' is, for example, greater than 10^6 ohm-cm. The semiconductor layer 14' is doped with an n-type dopant, such as silicon or sulphur, to have a donor concentration of about 10^{17} carriers per CM^3. The transistor device 10' has a pair of source electrodes 18' formed on and in ohmic contact with the upper surface of the semiconductor layer 14'. A portion of a drain electrode 20' is also disposed over the upper surface of the semiconductor layer 14', such a portion of the drain electrode also being formed in ohmic contact with the semiconductor layer 14'. The remaining portion of the drain electrode 20' is disposed on the surface of the substrate 12', as shown. Portions of a gate electrode 16' are formed over the semiconductor layer 14' and form Schottky barriers therewith, as shown. The remaining portions of the gate electrode 16' are disposed on the surface of substrate 12', as shown. The gate electrode 16' has a pair of fingers disposed between the source electrode 18' and the drain electrode 20', as shown.

Having formed gate, source and drain electrodes 16', 18' and 20', vias or holes 32, 34 and 36 are chemically etched from the bottom surface (i.e. from the surface of the semi-insulating gallium arsenide substrate 12') through the substrate 12' and the semiconductor layer 14' to expose bottom portions of the source electrodes 18, as shown, and through the substrate 12' to expose bottom portions of the gate and drain electrodes 16', 20', respectively, as shown. Bottom portions of the substrate 12', the sides of the vias or holes 32, 34, 36 and the exposed bottom portions of the gate, source and drain electrodes 16', 18' and 20' are covered with an evaporated conductive layer 38, here gold. The conductive layer 38 is then patterned into strips, as shown, using conventional photolithographic-chemicaletching techniques. The patterned conductive layer 38 is then increased in thickness (here to a total thickness of approximately 0.038 mm) by plating an additional layer of a suitable conductive metal 41, here gold, to form source, drain and gate contacts 40, 42, 44, as shown.

Referring now to Figures 5 and 6, a microstrip circuit 50 is shown to include three strip conductors 52, 54, 56, here gold, plated on a dielectric substrate 58, here beryllium oxide. As shown in Figure 6, a conductive layer 53, here gold, is plated on the bottom surface of the substrate 58 to provide a ground plane of the microstrip circuit 50. The edges 55 of the strip conductor 52 are electrically connected to the ground plane (i.e. the conductor 53) by plating around the sides of the dielectric substrate 58 with a suitable conductor 57, here gold. It is noted that the ends of the strip conductor 52 are flared to increase the length of the edges 55 being plated thereby, to provide good electrical connection to the ground plane conductor 53 by the plated conductor 57.

Referring now to Figures 7, 8 and 9, the field effect device 10' is electrically and mechanically connected to the microstrip circuit 50 by bonding (e.g. by soldering) the source, drain and gate contacts 40, 42, 44 onto the strip conductors 52, 54, 56, respectively, as shown. The source electrodes 18' are thus also electrically connected to the ground plane (i.e. the conductor 53) of the microstrip circuit 50, as shown. It is noted that the field effect device 10' is thus directly

bonded to th microstrip circuit 50 without the use of wire bonds.

Ref rring now to Figures 10, 11 and 12, a field effect transistor device 100 is sh wn t includ a plurality of field effect transistors connected in parallel. The device is adapted for use in relatively high power applications. In particular, the deivce 100 includes a semi-insulating, gallium arsenide substrate 112 and an epitaxially grown, n-type conductivity gallium arsenide semiconductor layer 114. The total thickess of the substrate 112 and the epitaxial layer 114 is here approximately 0.038mm. The device 100 has a plurality of, here three, source electrodes 118a, 118b, 118c formed in ohmic contact with the upper surface of the semiconductor layer 114. A portion of the drain electrode 120 is also disposed over the upper surface of the semiconductor layer 114. The drain electrode 120 is formed with finger-shaped drain electrodes 120a, 120b, which are in ohmic contact with portions of the semiconductor layer 114 disposed between adjacent pairs of the source electrodes 118a, 118, 118c. Thus, the drain electrode 120a is disposed between the source electrodes 118a and 118b, as shown, and the drain electrode 120b is disposed between the source electrodes 118b, 118c, as shown. The remaining portions of the drain electrode 120 are disposed on the substrate 112, as shown. A portion of the gate electrode 116 is formed over the semiconductor layer 114, with finger-shaped gate electrodes 116a, 116b, 116c, 116d disposed between the source electrodes 118a-118c and the drain electrodes 120a, 120b, as shown. In particular, gate electrode 116a is disposed between source electrode 118a and drain electrode 120a; gate electrode 116b is disposed between source electrode 118b and drain electrode 120a; gate electrode 116c is disposed between source electrode 118b and drain electrode 120b; and gate electrode 116d is disposed between source electrode 118c and drain electrode 120b, as shown. The gate electrodes 116a-116d form a rectifying metal-semiconductor contact (or Schottky barrier) with the semiconductor layer 114 as described above in connection with Figure 1. The remaining portions of the gate electrode 116 are disposed on the substrate 112, as shown.

Having formed the source electrodes 118a-118c, drain electrodes 120, 120a, 120b and gate electrodes 116, 116a-116d on the upper surface of the semiconductor layer 114, vias or holes 134a-134c are chemically etched from the bottom surface, (i.e. from the bottom surface of the semi-insulating, gallium arsenide substrate 112) through the substrate 112, and the semiconductor layer 114 to expose bottom portions of the source electrodes 118a, 118b, 118c. In addition, vias or holes 132 and 130 are chemically etched through the substrate 112 to exp s a bottom porti n of the gate electrod 116, and a bottom p r- tion of the drain electrode 120, as shown. Portions of the substrate 112, the sides of the vias r h les 134a;-34c, 132, and 130 and the exposed portions of the electrodes 118a, 118b, 118c, 116, and 120 are covered with an evaporated layer 138 of a suitable metal, here gold. The evaporated layer 138 is, after being patterned, as described above, then increased in thickness (here to a total thickness of approximately 0.038mm) by plating an additional layer of a suitable metal, here gold, to form the source, drain and gate contacts 120, 142, 144, as shown.

Ref rring now to Figures 13 and 14, a microstrip circuit 50' is shown to include three conductors, 52', 54', 56', formed on a dielectric substrate 58', here alumina. As shown in Figure 14, a conductive layer 53, here gold, is plated on the bottom surface of the substrate 58'. The conductive layer 53 is deposited into a surface of a gold plated copper carrier 55, as shown. The conductive layer 53 is then soldered to the carrier 55. A hole is then formed from the upper surface of the substrate 58' through such substrate 58' to the layer 53 (or to the carrier 55). The hole may be formed in any conventional manner, as by laser drilling. The hole is then filled with an electroplated copper conductive material 57 to provide good electrical and thermal conductivity to carrier 55. The conductive material 57, together with the conductive layer 53, provides the ground plane for the microstrip circuit 50'. The upper surface of the copper filling material 57 is then lapped to provide a smooth upper surface on the substrate 58'. The lapped copper surface is then gold plated to form the conductor 52'. The strip conductors 54', 56' are also formed, here also by gold plating, as shown in Figure 13. It follows, then, that conductor 52' is electrically connected to the ground plane of the microstrip circuit. Alternatively, the microstrip circuit 50 described in connection with Figures 4 and 6 may be used. As shown in Figures 15 and 16, the field effect device 100 is connected to the microstrip circuit 50' by disposing the source, drain and gate contact 140, 142, 144, respectively, on, and directly bonding them (here by soldering) to, the strip conductors 52', 54', 56', respectively, as shown. It is noted that th field effect device 100 is thus directly bonded to the microstrip circuit 50' without the use of wire bonding.

Figure 17 shows a plurality of field effect devices 100a-100c formed on separate substrates and connected in parallel to a microstrip circuit 150. Figure 18 shows a plurality of field effect devices 100a'-100c' formed on a single substrate and interconnected with a microstrip circuit 150'.

CLAIMS

1. A semiconductor device, comprising a substrate structure including a semiconductor, first and second electrodes in ohmic contact with the semiconductor, a third electrode for controlling the flow of charge carriers between the first and second electrodes, and two electrical conductors extending through the substrate structure, each electrical conductor being electrically connected to a corresponding one of two of the first, second and third electrodes.

2. A s miconductor device according to claim 1, including a third electrical conduct r ext nding through the substrate structure and being electrically connected to the remaining one of the first, second and third electrodes.

3. A semiconductor device according to claim 1 or 2, wherein the substrate structure includes a semi-insulating substrate supporting the semiconductor on one surface thereof, and wherein the electrical conductors extend through the semi-insulating

substrate.

4. A semiconductor device according to claim 1 or 2, wh rein the substrate structure includes a single crystal substrate with a semiconductor region therein.

5. A semiconductor device according to any one of claims 1 to 5, wherein there is a plurality of second electrodes and the third electrode has portions controlling the flow of charge carriers between the first electrode and the respective second electrodes, and wherein a plurality of the conductors extend through the substrate structure to the second electrodes respectively.

7. A semiconductor device according to any of claims 1 to 6, wherein a plurality of portions of the first and third electrodes are interdigitated with a plurality of the second electrodes, and wherein a plurality of the conductors extend through the substrate structure to the second electrodes respectively.

8. A semiconductor device according to any of claims 1 to 7, further comprising a microwave structure, including a dielectric substrate, a ground plane on one surface of the dielectric and having a contact region, two microstrip conductors having contact regions disposed on a second surface of the dielectric substrate, and wherein at least two of the said electrical conductors are disposed on and electrically connected to two of the contact regions.

9. A semiconductor device according to claim 8, insofar as dependent on claim 2, wherein the said third electrical conductor is electrically connected to the raminaing one of the contact regions.

10. A field effect transistor comprising a substrate structure including a semiconductor, source, drain and gate electrodes disposed on a surface of the semiconductor, and source, drain and gate electrodes extending through the substrate structure to the corresponding ones of the source, drain and gate electrodes.

11. A field effect transistor according to claim 10, further comprising a microwave structure including a ground plane on one surface of a dielectric substrate, and two microstrip conductors on the other surface of the dielectric substrate, the substrate structure and dielectric substrate being sandwiched together with the source, drain and gate conductors connected to contact regions, on the said other surface, of the ground plane and two microstrip conductors.

12. A semiconductor device substantially as hereinbefore described with reference to Figures 1 to 9 or Figures 1 to 9 as modified by Figures 10 to 12 or 13 to 17 or 17 or 18 of the accompanying drawings.

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